Engineering

Query paper:
Title: FinFET-a self-aligned double-gate MOSFET scalable to 20 nm
Abstract: MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped Si/sub 0.4/Ge/sub 0.6/ as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.

Candidate papers:

1. **Title:** Design and performance considerations for sub-0.1/spl mu/m double-gate SOI MOSFET'S
   Abstract: We present a simulation-based analysis of the device design and circuit performance trade-offs between short channel immunity and parasitic device capacitances of sub-0.1 /spl mu/m double-gate SOI MOSFET's. We demonstrate that perfect alignment of the bottom gate to the top gate is not necessary to achieve adequate short channel immunity but is required to maintain short gate delays. Double-gate MOSFET device design guidelines are provided.
2. **Title:** A folded-channel MOSFET for deep-sub-tenth micron era
   Abstract: Deep-sub-tenth micron MOSFETS with gate length down to 20 nm are reported. To improve the short channel effect immunities, a novel “Folded Channel Transistor” structure is proposed. The quasi-planar nature of this n~ ewvariant of the vertical double-gate SOI MOSFETS[1],[2] simplified the fabrication process. The special features of the structure (Fig. 1) are:(1) a transistor is formed in a vertical ultra-thin Si fin and is controlled by a double-gate, which suppresses short channel effects;(2) the two gates are self-aligned and are aligned to the S/D;(3) S/D is raised to reduce the parasitic resistance;(4) new low-temperature gate or ultra-thin gate dielectric materials can be used because they are deposited after the S/D; and (5) the structure is quasi-planar because the Si fins are relatively short.
3. **Title:** Impact of the vertical SOI'DELTA'structure on planar device technology
   Abstract: A fully depleted lean channel transistor (DELTA) with its gate incorporated into a new vertical ultrathin silicon-on-insulator (SOI) structure is presented. In the deep-submicrometer region, selective oxidation produces and isolates an ultrathin SOI MOSFET that has high crystalline quality, as good as that of conventional bulk single-crystal devices. Experiments and three-dimensional simulations have shown that this new gate structure has effective channel control and that the vertical ultrathin SOI structure provides superior device characteristics: reduction in short-channel effects, minimized subthreshold swing, and high transconductance.
4. **Title:** Monte Carlo simulation of a 30 nm dual-gate MOSFET: How short can Si go?
   Abstract: Monte Carlo simulation is used to explore the characteristics of an n-channel MOSFET at the presently perceived limits of scaling. This dual-gated 30 nm gate-length FET is found to have excellent characteristics for use in digital logic, including a transconductance as high as 2300 mS/mm and an estimated ring-oscillator delay of 1.1 ps. The various motivations for this device design are discussed, illuminating the reasons for claiming that it is at the limits of scaling.

5. **Title:** A New Scaling Methodology For The 0.1 - 0.025/spl mu/m MOSFET
   Abstract: In this work a MOSFET structure with an undoped ultra-thin epitaxial layer over an heavily doped substrate is compared to an uniformly doped MOS (2 x 10^18), a buried channel MOS and two SOI structures (Fig. 1). The first (SOI-S) is made of an ultra-thin undoped Si layer (10 nm) over a 50 nm thick oxide layer. The second one (SOI-D) is a double gate structure with a silicon layer 10 nm thick. Extremely shallow LDD-type source/drain profiles are adopted for all the considered structures.
6. **Title:** Reliable tantalum gate fully-depleted-SOI MOSFETs with 0.15 /spl mu/m gate length by low-temperature processing below 500/spl deg/C
   Abstract: A reliable tantalum (Ta) gate device technology, which can drastically reduce the number of process steps, has been developed. Ta gate Fully-Depleted-Silicon-On-Insulator (FDSOI) MOSFETs with 0.15 /spl mu/m gate length by low-temperature processing below 500/spl deg/C after the gate oxide formation have good on/off characteristics. Comprehensive design guidelines for Ta gate MOSFETs in the deep-submicron regime are provided by investigating a wide range of performance and reliability constraints on the process temperature and the SOI thickness. For low-temperature processing, there is the lower limit of the SOI thickness which is given by the recrystallization of the source/drain layer.

Exemplary analysis:

1. **Relevance:** The query paper proposes a novel FinFET design to suppress short channel effects, making the cited paper's analysis of short channel immunity directly relevant. The discussion on the necessity of gate alignment might also provide a contrasting or supporting viewpoint to the FinFET's self-aligned gate approach.
   Reason for Citation: This paper is likely cited because it discusses the trade-offs between short channel immunity and parasitic device capacitances in sub-0.1 μm double-gate SOI MOSFETs.
2. **Relevance:** The "Folded Channel Transistor" structure shares similarities with the FinFET in terms of addressing scaling challenges and suppressing short channel effects. The quasi-planar nature and the mention of a double-gate controlled transistor align with the FinFET's design principles, making this citation relevant for background and comparison.
   Reason for Citation: The citation of this paper could be due to its introduction of a novel structure to improve short channel effect immunities, similar to the FinFET's goal.
3. **Relevance:** Since the FinFET also utilizes a vertical gate structure to achieve its performance improvements, the cited paper's findings on vertical SOI structures provide a foundational understanding of the advantages and technological implications of such designs.
   Reason for Citation: This paper is likely cited for its discussion on the vertical ultrathin SOI structure's benefits, such as reduced short-channel effects and high transconductance.
4. **Relevance:** The FinFET design is proposed as scalable to 20 nm, and the cited paper's simulation results for a 30 nm dual-gate MOSFET offer insights into the performance characteristics and scaling limitations of closely related technology. This comparison could help justify the FinFET's design choices and scalability.
   Reason for Citation: The citation of this paper could be due to its use of Monte Carlo simulation to explore the limits of scaling in silicon-based MOSFETs.

5. **Relevance:** The comparison of different MOSFET structures and the focus on scaling methodologies are directly relevant to the FinFET's design and its scalability to 20 nm. The discussion on ultra-thin layers and doping profiles could provide essential background and justification for the FinFET's structural choices.
   Reason for Citation: This paper is cited probably because it presents a scaling methodology for MOSFETs, comparing various structures including a double gate SOI design.
6. **Relevance:** The paper provides design guidelines and performance/reliability constraints that could be applicable or contrasted with the FinFET's approach, especially considering the use of boron-doped Si/Ge as a gate material in the query paper.
   Reason for Citation: The citation of this paper might be due to its focus on low-temperature processing for Ta gate FDSOI MOSFETs, which is relevant for the FinFET's fabrication process.

Exemplary ranking: Ranked order: paper 1, paper 2, paper 3, paper 4, paper 5, paper 6

1. **Explanation:** This paper is directly relevant because it addresses the core issue of short channel effects that the FinFET design aims to suppress. Its focus on double-gate SOI MOSFETs makes it highly pertinent for understanding the design considerations and performance metrics that are critical for the development of FinFET technology.
2. **Explanation:** The novel structure proposed in this paper for improving short channel effect immunities aligns closely with the objectives of the FinFET technology. The similarities in addressing scaling challenges and the focus on a quasi-planar, double-gate approach make this paper crucial for understanding alternative or complementary design strategies.
3. **Explanation:** Given the FinFET's utilization of a vertical gate structure, this paper's insights into the advantages and technological implications of vertical SOI structures are invaluable. It provides a foundational understanding that is necessary for appreciating the benefits and potential of vertical integration in semiconductor devices.
4. **Explanation:** This paper's exploration of scaling limits through Monte Carlo simulation is directly relevant to the scalability aspect of FinFET technology. Understanding the performance characteristics and limitations at the nanoscale is essential for advancing FinFET design and justifying its scalability to 20 nm.
5. **Explanation:** The focus on scaling methodologies and the comparison of different MOSFET structures, including double-gate designs, provides critical context for the FinFET's scalability and design choices. This paper offers essential background and justification for structural decisions in FinFET technology.
6. **Explanation:** While this paper is relevant for its focus on fabrication processes, particularly low-temperature processing, it might be considered less directly related to the core themes of the FinFET design compared to the other papers. However, it still provides valuable insights into design guidelines and performance/reliability constraints that could influence FinFET fabrication.